IN THE SPECIFICATION

Please amend the specification as follows. Paragraphs that are being amended are listed in their entirety; changes are indicated in the left margin with a vertical change bar. Deletions are marked by ~~strikethrough~~; insertions are underlined.

Please amend the paragraph on page 28, line 16 through page 29, line 14, as follows:

Figure 16 shows the application of processing in accordance with the invention to routing product in a chip fabrication manufacturing system (chip fab). For purposes of illustration, five machines are indicated in connection with Figure 16, represented by Machine A1, Machine A2, ..., Machine A5. Zernike distortion data collected in accordance with the methods described above for the five machines shown is provided to a comparator shown in Figure 16. The comparator can be implemented as a software operation or application that is executed on the imaging projection system machine ~~(see, for example, Reference 183)~~. That is, the imaging projection system machine can include a computer that controls operations of the system and that implements the comparator functionality. The computer can comprise a desktop computer, workstation, or processor and associated apparatus that is integrated into the system and can provide the comparator functionality. After the comparator receives the Zernike distortion data, the comparator creates a routing preference list. The routing preference list shows which machines are best suited to work with other machines, as far as minimizing lens induced distortion is concerned. Thus, from the exemplary Figure 16 output of the comparator when Machine A1 prints Layer 1, it should be apparent that, in decreasing order of preference, Layer 2 should be printed on Machines A1, A5, A3, A2, A4. Each of the other machines will have a corresponding routing preference list. The routing preference lists, generated in accordance with Zernike distortion data collected in

accordance with the methods described above, will be used by the chip fab to control routing of materials and manufacturing of circuit chips during processing, as will be known to those skilled in the art in view of the description above.